Indian Institute of Information Technology Sri City (IIIT Sri City)

M.Tech VLSI

Type Pg Program	Mode Online
Duration 2 Years	Total fees ₹ 271,000

UNIVERSITY

Indian Institute of Information Technology Sri City (IIIT Sri City)

The Indian Institute of Information Technology Sri City, Chittoor is an Institute of National Importance established through a public-private partnership. Known for its industry-oriented curriculum, research focus and technology-driven learning, the institute prepares professionals to address emerging digital challenges. IIIT Sri City promotes innovation, entrepreneurship and interdisciplinary collaboration to develop globally competent technology leaders.

PROGRAM

M.Tech VLSI

Highlights

- Earn an M.Tech degree in VLSI from IIIT Sri City through an online learning format.
- Build expertise across semiconductor physics, digital and analog VLSI design, SoC and low-power technologies.
- Gain hands-on exposure to Verilog HDL, simulation labs and industry-relevant VLSI design tools.
- Learn from experienced IIIT Sri City faculty and industry experts through an application-oriented curriculum.
- Participate in campus immersion opportunities and gain IIIT Sri City alumni status upon successful completion.

Learning outcomes

- Explain semiconductor-device principles and their role in advanced VLSI systems.
- Design and simulate digital, analog and mixed-signal integrated circuits.
- Apply low-power design approaches to improve system performance and energy efficiency.
- Evaluate VLSI systems using appropriate testing, fault-modelling and reliability techniques.
- Conduct independent research and develop solutions for advanced VLSI design challenges.

Eligibility Criteria

Applicants should have a B.Tech / BE /BS/ M.Tech / MSc (4 semester program) / MCA (4-semester program) / MS Degree (min. 4 semester) / equivalent degree in the relevant discipline with at least 55% marks or 5.5/10 CPI. In the case of the candidate belonging to SC, ST, or Persons with Disability (PwD) category, this is relaxed to 50% or equivalent 5.0 CGPA/CPI

For MCA/MSC passed graduates, the percentage score of MCA/MSC would be considered. For BE/BTech Engineering graduates without PG specialization, the percentage score of the undergraduate degree would be considered. For a post-graduation in the Engineering field of study,

PG score qualification can be considered.

GATE is not mandatory.

Selection process will be scheduled post-counseling & application process, depending on the number of eligible applications as per seat availability for the program. This entire process will be online.

Candidates who do not meet the minimum CGPA or percentage requirement, can still be considered if they provide relevant work experience in the technical field.

Curriculum Overview (continued)

Semester I (28 subjects)

- Semiconductor Device Physics
- Semiconductor Properties and Band Structure
- Diode Modelling
- MOS Modelling
- Quantum Physics Aspects of Device Modelling
- Introduction to Quantum-Effect Device Modelling
- Nanoscale Transistors
- VLSI Technology
- Introduction to VLSI Technology
- Oxidation
- Diffusion and Ion Implantation
- Epitaxy and Thin-Film Deposition
- Etching
- Lithography
- Digital VLSI Circuit Design
- Review of MOSFET Operation
- CMOS Inverter
- Combinational Logic
- Sequential Logic
- Memories and Array Structures
- Timing Fundamentals
- Verilog HDL
- Overview of Digital Design with Verilog HDL
- Gate-Level Modelling
- Dataflow Modelling
- Behavioural Modelling
- Structural Modelling
- Timing Delays and Switch-Level Modelling

Curriculum Overview (continued)

Semester II (28 subjects)

- Analog VLSI Design
- Analog and Mixed-Signal VLSI
- Single-Stage Amplifiers
- Current Mirrors and Biasing Techniques
- Frequency Response of Amplifiers
- Feedback
- Operational Amplifiers
- Low-Power VLSI Design
- Introduction to Low-Power VLSI
- Simulation-Based Power Analysis
- Near-Threshold Digital CMOS Circuits
- Circuit-Level Low-Power Design
- Low-Power Architectures and Systems
- Low-Power Clock Distribution
- System on Chip
- Introduction to System on Chip
- Digital Logic and On-Chip Communication for SoCs
- Embedded Processors and Microcontroller Architectures
- Memory Systems and Storage
- Hardware–Software Co-design
- SoC Design Tools
- VLSI System Design
- Minimisation and Transformation of Sequential Machines
- Digital Design Using Programmable Logic Devices
- Introduction to Static Timing Analysis
- Introduction to Placement and Routing
- Memory Units
- Design Abstraction

Curriculum Overview (continued)

Semester 3 (23 subjects)

- Mixed-Signal Circuit Design
- Signals
- Filters and Tools
- Sampling and Aliasing
- Analog Filters
- Digital Filters
- Data-Converter Signal-to-Noise Ratio
- Data Converters
- Nano-Scale Devices
- Quantum Transport and Carrier Dynamics
- MOSFETs and Bipolar Devices
- Nanoscale MOSFETs and Ballistic Transport
- MOSFETs with Scattering Effects
- Nanowire and Carbon-Nanotube FETs
- Molecular and Single-Electron Transistors
- VLSI Testing and Testability
- Fundamentals of Testing and Faults
- Fault Modelling and Test Patterns
- Combinational Circuit Fault Diagnosis
- Sequential Circuit Testing and Built-In Self-Test
- Memory Faults and Testing Techniques
- PLA Design and Fault Testing
- Seminar

Curriculum Overview (continued)

Semester IV (1 subject)

- Dissertation

Fee Structure

Fee heads	Year 1	Year 2	Total
Program Fee	₹ 132,000	₹ 132,000	**₹ 264,000**
Application Fee	₹ 5,000	—	**₹ 5,000**
Administration Fee	₹ 2,000	—	**₹ 2,000**
Total	**₹ 139,000**	**₹ 132,000**	**₹ 271,000**